Data Book
ZF 104Card/EV

PC104 CPU Board based on the *OEMmodule™*

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General Description

The ZF 104Card/EV is a full-featured embedded system computer utilizing the ZF MicroSystems OEMmodule. It is a complete PC/AT-compatible motherboard including standard peripheral interfaces. Its small size, low power consumption, and rugged construction makes it ideal for embedded systems. You can develop software directly on a 104Card/EV system or on a desktop PC/AT and transfer your code directly to an OEMmodule-based embedded system with little or no modification.

The 104Card/EV includes all standard motherboard functions, serial and parallel I/O, floppy and EIDE disk controllers, a high-performance CRT/flat-panel video controller, a 10BaseT Ethernet interface, an internal resident Flash disk for program storage, PC/104 expansion bus, and a standard PC/AT BIOS.

For many systems, the standard PC ROM-BIOS and resident Flash disk eliminate the need for rotating media (such as a floppy or hard disk) for application program storage.

INDUSTRY STANDARD COMPATIBILITY

The 104Card/EV expansion bus conforms to the popular PC/104 standard. It allows you to easily integrate a wide variety of low-cost PC/104 peripherals in your embedded system.

The board's PC-compatible serial ports, parallel port, floppy interface, and hard disk interface allow you to use standard hardware, cables, and software libraries in your development program.

Features

100 MHz 486SX CPU

- Full 32-bit internal architecture, cost-effective 16-bit external bus.
- Virtual memory, paging, and hardware-enforced protection.
- Physical memory space up to 18 MB.

PC Core Logic

- AT-compatible DMA controllers, interrupt controllers, timer/counters .
- AT keyboard controller.
- Real-time clock.

DRAM Controller

- High performance MUXed DRAM interleave, CPU pipelined operation.
- 2MB DRAM in the OEMmodule and 16MB additional DRAM soldered on board.
- Shadowed BIOS for optimum performance.

Serial Ports

- Two 16550-compatible serial ports – one dedicated RS232 and one optional RS232/RS485.

Parallel Ports

- A fully-compatible PC/AT parallel port, plus bi-directional operation (EPP)

Floppy Disk Controller

- Software compatible with 765B floppy controller and PC BIOS.
- Integrated digital data separator capable of data transfer rates up to 2Mbps.
- Supports all standard PC floppy formats
- Only supports one floppy drive
- FFC connector provided for drive connection.

EIDE Hard Drive Interface

- Standard 40-pin interface to EIDE hard disk drive.
- Supports up to two EIDE drives (master/slave).
- Supports CompactFlash™.

CRT/Flat-Panel Controller

- Based on Chips and Technologies 65545 Flat Panel/CRT GUI accelerator
- 512K byte video memory
- Fully compatible with VGA standard
- Hardware windows acceleration
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768 x 16 colors and 800 x 600 x 256 colors
- True-color and Hi-color display capability with flat panels and CRT monitors up to 640 x 480
- Direct interface to color and monochrome Dual Drive (DD) and Single Drive (SS) STN and TFT panels.
- Supports 8 to 24-bit data interfaces.
- Supports power-sequencing controls for Vdd, Vee, and +12V to inverter for backlights
- Flat-Panel (3.3V and 5.0V) support with add-on daughter card (optional)

Ethernet Controller

- 10BaseT (twisted-pair), 10M bit/s
- Supports IEEE 802.3 (ANSI 8802-3) and Ethernet standards
- Based on the Realtek RTL8019AS full duplex Ethernet controller with Plug and Play function
- Supports full duplex operation on the 10BaseT and AUI ports
- LNKST and RCV LEDs for line verification
- Boot PROM capability for booting from network
- Supports Microsoft's Plug and Play System configuration
- Broad NOS support, including Novell Netware, Microsoft Windows 95, Microsoft LAN Manager, SCO UnixWare, IBM LAN Server, SunSoft PC-NFS, SunSoft Solaris, Artisoft LANtastic, Banyan Vines

Solid-State Flash Storage

- 2MB Internal Flash Memory.
- 1.4MB resident flash disk(RFD) available for DOS and OEM software use.
- Expandable by adding 2MB to 60MB of CompactFlash.

PC BIOS

- Standard AT BIOS functionality.
- Easy to upgrade using ZF MicroSystem's unique Download Interface.
- Setup information is stored in non-volatile Flash EPROM. Allows battery-free operation.

Expansion Bus

- Compliant with standard PC/AT expansion bus with an IRQ and DMA channel subset
- 104Card/EV is a non-stackthrough version
- Add up to three PC/104 modules

Power Monitor

- Brownout protection, provides reliable reset signal if power fluctuates.
- Resistor-configurable voltage threshold.

Electrical Specifications

- Requires +5VDC @ 850 mA ±5% (2 MB internal DRAM).
- Future support for low-power modes.

Mechanical Specifications

- 3.6" x 3.8" x 1.0"(91.6mm x 96.7mm x 25.4mm)
- PC/104 bus compliant with PC/104 V2 specification.
- Standard ribbon cable connectors for EIDE, serial, and parallel interfaces. FFC cable required for floppy.

Environmental Specifications

- Operating temperature: 32F to 158F (0C to 70C).
- Storage temperature: -67F to 185F (-55C to 85C).
- Weight: 4 oz (113.5 gm).

Contents

ORDERING INFORMATION

104-4EV-Q-01 — ZF PC104Card 486, ETH/VGA, 100MHz with 18M byte DRAM, 2MB built-in Flash, CompactFlash socket, 2 serial and 1 parallel port, speaker, and BIOS. Does not include manuals, utility disk, or cables.

104-4EV-K-01 — ZF PC104Card 486,ETH/VGA Development Kit, 100MHz with 18M byte DRAM, 2MB built-in Flash, CompactFlash socket, 2 serial and 1 parallel port, speaker, BIOS, technical manuals, cables, and utility software.

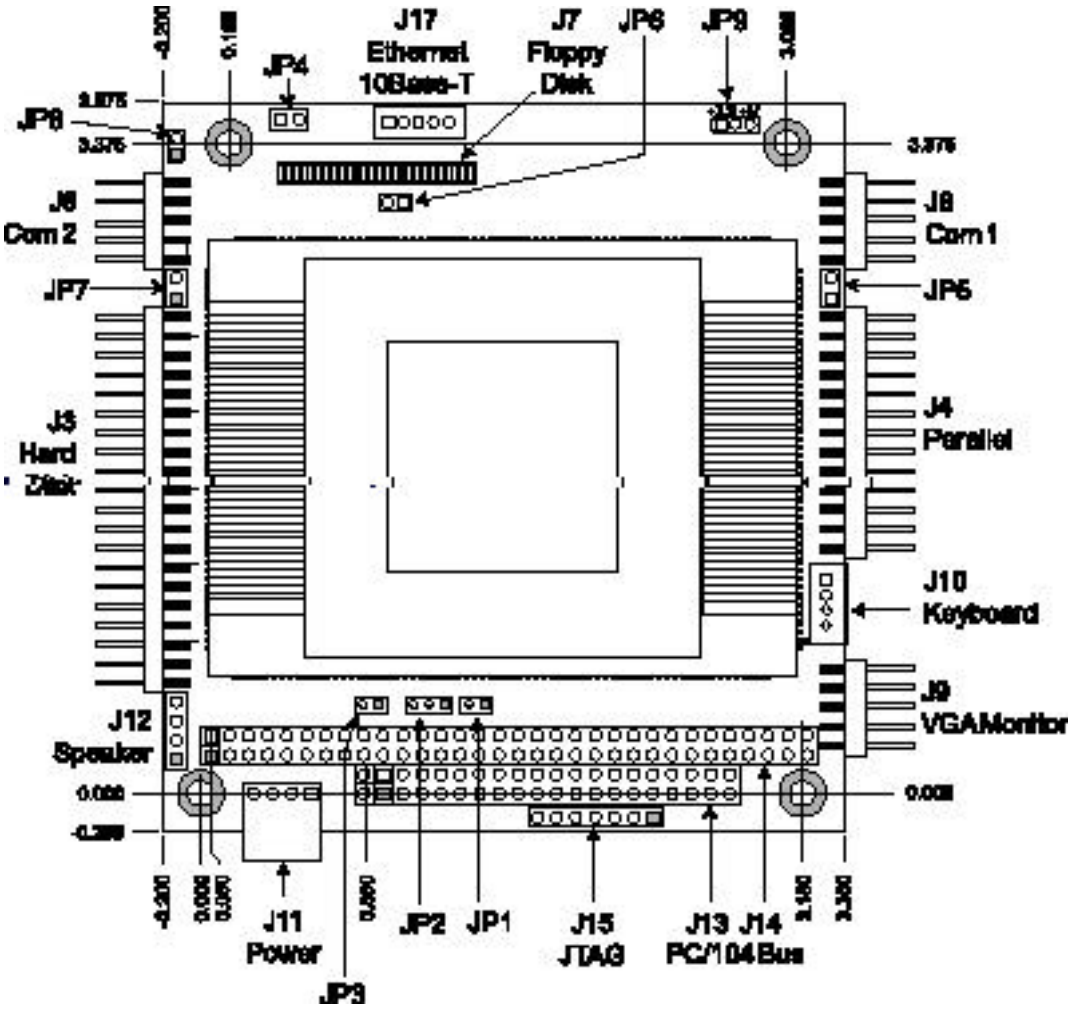

Figure 1. Board Dimensions

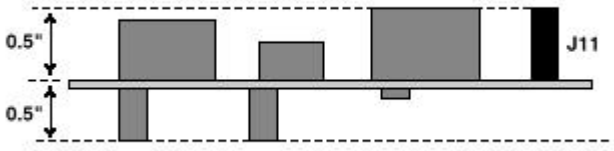

Figure 2 Height Dimension

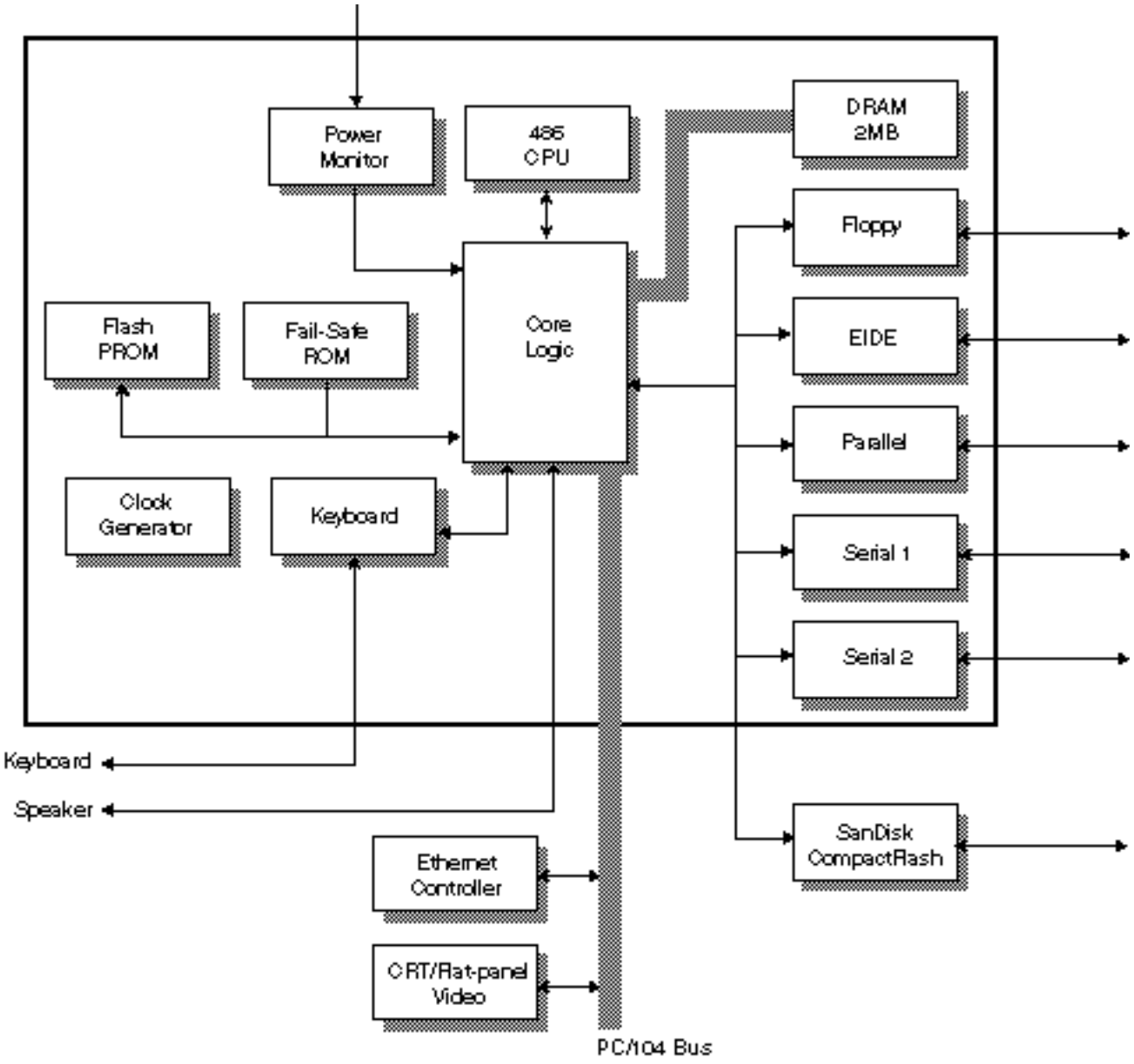

Figure 3. System Block Diagram

Connector Summary

Table 1 summarizes the use of J1 through J17.

Connector	Function	Type
J1	Flat Panel I/F 2	30-Pin Dual Row, 2mm centers
J2	CompactFlash Socket	50-Pin CompactFlash Card Header
J3	EIDE	40-Pin Dual Row, .100 centers
J4	Parallel 1	26-Pin Dual Row, .100” centers
J5	Flat Panel I/F 1	24-Pin Dual Row, 2mm centers
J6	Serial 1	10-Pin Dual Row, .100” centers
J7	Floppy	26-Pin ZIF FFC connector
J8	Serial 2	10-Pin Dual Row, .100” centers
J9	VGA	10-Pin Dual Row, .100” centers
J10	Keyboard	4-Pin Single Row, .100” centers
J11	Power	4-Pin PC Floppy Power
J12	Speaker	4-Pin Single Row, .100” centers
J13	PC/104 C/D	40-Pin Dual Row, .100” centers
J14	PC/104 A/B	64-Pin Dual Row, .100” centers
J15	Reserved	7-Pin Single Row, .100” centers
J17	10BaseT Ethernet	5-Pin Single Row, 2mm centers

Table 1. Connector Summary

Jumper Summary

The 104Card/EV provides a number of jumper options to configure features on the board. The jumpers, labeled "JP*n*", are configured with 2mm shorting blocks. Table 1 shows a summary of the jumpers, their functions, and the factory default settings. For jumper options with more than two pins, default shorted pin-pairs are listed as *n1*/*n2*.

Jumper	Function	Default
JP1	CompactFlash Type On=M-Systems	Off
JP2	Compact Flash Master/Slave 1/2=Master, 2/3=Slave	1-2
JP3	VBATT	Off
JP4	Reset (external reset connection; a ground on pin 1 resets the system)	Off
JP5	Keyboard Lock	Off
JP6	Backup Fail Safe BIOS (BDIS-) On=Fail-Safe ROM, Off=Flash BIOS	Off
JP7	HDD LED	Off
JP8	Watchdog Timer	On
JP9	Flat-Panel Signal Levels 1/2=3.3V, 2/3=5V	1-2

Table 2. Jumper Summary

DRAM Interface

The 104Card/EV is supplied with 2M bytes of DRAM which is internal to the OEMmodule. The 104Card/EV also has 16M bytes of DRAM which is soldered on the board.

SETTING MEMORY SIZE

The BIOS automatically senses the amount of memory installed in your system and displays that information on the Setup configuration page. There is no user setting.

Power and Utility Connector

+5 Volt and +12 Volt power are supplied through the 4-pin connector, J11.

+5 Volts is used for the board's main logic supply. The pinout of this connector matches the pinout found on standard floppy disk drives, hard disks, and other such devices. Standard PC power supplies can be used without special cables.

+12V may be required if you connect a flat-panel display to a flat-panel daughter card mounted on J1 and J5.

Table 3 lists the power pins on J11.

Pin	Description
1	+5 Volts
2	Ground
3	Ground
4	+12 Volts

Table 3. Power Connector, J11

KEYBOARD

The 104Card/EV provides the standard keyboard signals on connector J10. Table 4 shows how to wire a DIN-6 connector for a standard PS/2 keyboard cable.

Signal Name	Pin	Function	6-Pin DIN
KBClock	1	Keyboard Clock	5
Power	2	+5 Volts	4
KBData	3	Keyboard Data	1
Ground	4	Ground return	3

Table 4. Keyboard Connector, J10

SPEAKER

Small piezoelectric speakers or standard PC speakers (with an 8 ohm coil) can be directly driven by the 104Card/EV through connector J12. The port supplies approximately 0.1 watt to the speaker. The speaker signal is TTL, current-limited with a series 33 ohm resistor. High frequencies are rolled off with a 0.01 µF capacitor (to ground).

Table 5 shows the pinout of J12.

Signal Name	Pin	Description
Speaker +	1	+5 Volts
Speaker -	2	Signal
GND	3	Ground
Speaker -	4	Signal

Table 5. Speaker Connector, J12

REAL-TIME CLOCK BATTERY

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time, date, and CMOS memory values when power is off. Connect the battery to JP3-1 to JP3_2 (Ground).

If the battery is not present or fails and +5 Volt power is removed, the RTC will lose the current time and date, but the Setup data will remain intact. CMOS configuration information is always read from a Flash EPROM copy (inside the OEMmodule) if there is a fault detected in the contents of the Setup parameters stored in the CMOS RAM portion of the RTC. For more information on the real-time clock, see the OEMmodule 486 databook.

Serial Ports

The 104Card/EV provides two full-featured PC-compatible asynchronous RS232C serial ports. The serial ports are treated as COM1 and COM2 by DOS. COM2 can optionally be configured as a RS485 port.

Standard system resources are allocated to the serial ports, as shown in Table 6:

Serial Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Serial 1	J6	COM1	3F8h–3FFh	IRQ4 (shared)
Serial 2	J8	COM2	2F8h–2FFh	IRQ3 (shared)

Table 6. Serial Port Resources

RS232 SERIAL PORT CONNECTORS

The RS232 serial ports (Serial 1 and Serial 2) are brought out to 10-pin dual-row ribbon-cable connectors J6 and J8. The connector pins are arranged to make it easy to construct a simple straight-through ribbon cable to a panel-mount DB-9 connector.

A full complement of input and output handshaking lines are implemented. Signals are at standard RS232C levels. Power for the RS232 voltage levels (-9V > x > +9V) is converted on-board from the +5V supply.

Pinouts for the serial connectors and for standard DB-9 connectors are shown in Table 7.

J6 and J8	DB-9 Pin	Signal	Function	In/Out
1	1	DCD	Data Carrier Detect	Input
3	2	RXD	Receive Data	Input
5	3	TXD	Transmit Data	Output
7	4	DTR	Data Terminal Ready	Output
9	5	GND	Signal Ground	
2	6	DSR	Data Set Ready	Input
4	7	RTS	Request To Send	Output
6	8	CTS	Clear To Send	Input
8	9	RI	Ring Indicator	Input
10		N/C	Ground	

Table 7. Serial Port RS232 Connectors, J6 and J8

J8	Signal
4	B
5	A

Table 8. Serial 2 RS485 Connections

Serial 1 is always enabled and requires no set up.

Serial 2 can be ENABLED/DISABLED via the Custom Setup Screen in the CMOS setup. COM2 operating mode can be configured as RS232 or RS485 in the Custom Setup Screen. Options for Serial2 interrupts can be selected in the Custom Setup Screen. The options are IRQ3,IRQ4 and DISABLED.

SERIAL PORT INTERRUPT SHARING

The COM1 and COM2 serial port interrupt request lines comply with the interrupt sharing scheme described in the PC/104 Version 2.3 specification. For a copy of the PC/104 Version 2.3 specification, visit the PC/104 Consortium web site (www.controlled.com/pc104). This sharing scheme is described in the OEMmodule Data Book.

The interrupt request lines from Serial 1 and Serial 2 are internally buffered in the OEMmodule with open collector buffers and internally connected to inputs IRQ4 and IRQ3 respectively. Internal 1000 ohm termination resistors hold the interrupt signals at logic 0 until an interrupt occurs. Other interrupt sources can be wire-ORed with either of these IRQ lines as long as they also follow the PC/104 interrupt sharing convention. The interrupt request signals appear on the PC/104 bus.

Note: The 1000 ohm pull-down resistor for each interrupt is provided on the board. Do not attach an external pull-down resistor.

Parallel Port

The 104Card/EV parallel port is fully compatible with the PC/AT parallel port. In extended mode, it functions as a PS/2-style bi-directional port.

The parallel port uses the following PC resources (Table 9):

Parallel Port	Connector	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	J4	LPT1	378h – 37Fh	IRQ7

Table 9. Parallel Port Resources

PARALLEL PORT SIGNALS

The parallel port output signals provide up to 48 mA drive current (active low). .0022 µF capacitors are connected from each data line to ground for noise suppression.

PARALLEL PORT REGISTERS

Table 10 summarizes the parallel port register interface. In this table, “A” indicates the port’s base address, for example, 378h.

Register	Bit	Signal Name	In/Out	Active High/Low
Data (A+0)	0	PD0	I/O	High
	1	PD1	I/O	High
	2	PD2	I/O	High
	3	PD3	I/O	High
	4	PD4	I/O	High
	5	PD5	I/O	High
	6	PD6	I/O	High
	7	PD7	I/O	High
Status (A+1))	0	1	-	-
	1	1	-	-
	2	1	-	-
	3	ERR-	In	Low
	4	SLCT-	In	High
	5	PE	In	High
	6	ACK-	In	High
	7	BUSY	In	Low
Control (A+2)	0	STRB-	Out	Low
	1	AUTOFD-	Out	Low
	2	INIT-	Out	High
	3	SLIN-	Out	Low
	4	IRQ ENABLE	-	High
	5	1	-	-
	6	1	-	-
	7		-	-

Table 10. Parallel Port Registers

The parallel port signals appear on J4, a 26-pin dual-row ribbon-cable connector. The port may be cabled to appear as a standard PC DB-25 connector.

Table 11 shows the parallel port signals that appear on J4 and the equivalent pinout on a DB-25S connector.

J3	DB-25 Pin	Signal	Function	In/Out
1	1	STRB-	Output Data Strobe	Output
2	14	AUTOFD-	Auto Feed	Output
3	2	PD0	Data Bit 0	I/O
4	15	ERR-	Printer Error	Input
5	3	PD1	Data Bit 1	I/O
6	16	INIT-	Initialize Printer	Output
7	4	PD2	Data Bit 2	I/O
8	17	SLIN-	Selects Printer	Output
9	5	PD3	Data Bit 3	I/O
10	18	GND	Signal Ground	N/A
11	6	PD4	Data Bit 4	I/O
12	19	GND	Signal Ground	N/A
13	7	PD5	Data Bit 5	I/O
14	20	GND	Signal Ground	N/A
15	8	PD6	Data Bit 6	I/O
16	21	GND	Signal Ground	N/A
17	9	PD7	Data Bit 7	I/O
18	22	GND	Signal Ground	N/A
19	10	ACK-	Character Acknowledged	Input
20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer Busy	Input
22	24	GND	Signal Ground	N/A
23	12	PE	Out Of Paper	Input
24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer Selected	Input
26	N/A	GND	Signal Ground	N/A

Table 11. Parallel Port Connector, J4

PARALLEL PORT CONFIGURATION

The parallel port, LPT1, appears at address 378h. It is connected, by default, to IRQ7. The interrupt can be disabled in the Custom Setup Screen in CMOS Setup. The port can be configured as output-only, bi-directional, EPP, or DISABLED by choosing one of options in the Custom Setup Screen in CMOS Setup.

Floppy Interface

A PC-compatible floppy drive interface is supplied on J7. In PC-compatible systems, the BIOS and DOS support two drives configured as Drive A: and Drive B:. These are configured using the BIOS Setup function. The 104Card/EV only supports one physical floppy drive.

Table 12 shows the PC resources used by the floppy subsystem.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2–DACK2	DMA Controller Channel

Table 12. Floppy Interface Resources

The floppy drive interface supports the standard PC floppy disk formats, 360K, 1.2M, 720K, 1.44M, and 2.88M. You must specify the type of drive connected to the floppy interface in the BIOS CMOS Setup. Press <Del> during the Power-On Self Test (POST) to enter Setup. The first drive typically appears to DOS as drive A:, and the second drive as B:.

The floppy drive is connected to the 104Card/EV using a 26 pin FFC cable. The TEAC FD-05HG floppy drive is pin compatible with the 104Card/EV floppy interface.

Note: The board's internal Resident Flash Disk, if enabled, can be configured as drive A and any floppy disk drive configured as drive A will become Drive B automatically. Only two floppy drives (A and B) are supported.

Table 13 lists the signals on the J7 floppy interface.

J7 Pin	Signal Name	Function	In/Out
2	INDEX-	Index Pulse	In
4	DRV0-	Drive Select 1	Out
6	DSKCHG-	Disk Change	In
8	N/C	N/A	
10	MTR0-	Motor On 0	Out
12	DIR-	Direction Select	Out
14	STEP-	Step Pulse	Out
16	WDATA-	Write Data	Out
18	WGATE-	Write Gate	Out
20	TRK0-	Track 0	In
22	WRPRT-	Write Protect	In
24	RDATA-	Read Data	In
26	HDSEL-	Head Select	Out
1,3,5	+5 volts	+5 volts	
7-13 (odd)	N/C	N/A	
15-25 (odd)	Ground	Ground	

Table 13. Floppy Drive Connector, J7

EIDE Interface

The 104Card/EV is supplied with a standard EIDE Hard Disk Interface at connector J3. This is the standard interface used in PC-compatible systems for hard disk drives, CD-ROM drives, and certain other peripherals.

Up to two drives can be connected in a master-slave arrangement. Generally, the first hard disk drive (master drive) will appear as the C drive to DOS. The second drive (slave drive), if attached, will appear as drive D.

If you use a CompactFlash, it is installed as an IDE drive in the system. Like an actual IDE drive, you can jumper the CompactFlash to be a master or slave. Configure your IDE drive appropriately.

Table 14 lists the resources used by the EIDE interface.

Resource	Function
I/O Address 1F0h-1F7h	Hard Disk Interface
IRQ14	Interrupt

Table 14. EIDE Interface Resources

Use Setup to enable your attached hard drives. You must match the drive parameters in Setup with the actual parameters of your connected drive(s).

EIDE drives are typically attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard 0.1 inch-spacing connector and the smaller connector on the drive. These generally are supplied with the drive.

The pinout for the EIDE interface, J3, is shown in Table 15.

Note: Due to drive manufacturer's different implementations of the master/slave arrangement, it may not be possible to properly configure two IDE drives from different sources to share the EIDE bus.

J3 Pin	Signal Name	Function	In Out	J3 Pin	Signal Name	Function	In Out
1	HDRESET-	Reset signal from host	OUT	21	N/A	Reserved	N/C
2	GND	Ground		22	GND	Ground	
3	HDD07	Data bit 7	I/O	23	HDIOW-	Write strobe	OUT
4	HDD08	Data bit 8	I/O	24	GND	Ground	
5	HDD06	Data bit 6	I/O	25	HDIOR-	Read strobe	OUT
6	HDD09	Data bit 9	I/O	26	GND	Ground	
7	HDD05	Data bit 5	I/O	27	RSVD	Reserved	N/C
8	HDD10	Data bit 10	I/O	28	HDALE	Address latch enable	OUT
9	HDD04	Data bit 4	I/O	29	RSVD	Reserved	N/C
10	HDD11	Data bit 11	I/O	30	GND	Ground	
11	HDD03	Data bit 3	I/O	31	IRQ14	Drive interrupt request	IN
12	HDD12	Data bit 12	I/O	32	IOCS16-	I/O Chip Select 16	In
13	HDD02	Data bit 2	I/O	33	HDA1	IDE Address 1	Out
14	HDD13	Data bit 13	I/O	34	RSVD	Reserved	N/C
15	HDD01	Data bit 1	I/O	35	HDA0	IDE Address 1	Out
16	HDD14	Data bit 14	I/O	36	HDA2	IDE Address 2	Out
17	HDD00	Data bit 0	I/O	37	HDCS0-	IDE Chip Select 0	Out
18	HDD15	Data bit 15	I/O	38	HDCS1-	IDE Chip Select 1	Out
19	GND	Ground		39	LEDIN-		
20	KEY	Keyed pin	N/C	40	GND	Ground	

Table 15. EIDE Drive Connector, J3

SVGA CRT/Flat-Panel Video Controller

The 104Card/EV provides a CRT/Flat-Panel video controller, based on the Chips and Technology 65545 Flat-Panel VGA controller. It is hardware-level register compatible with existing PC video standards. It supports CRT-only and flat panel-only display modes.

The controller is equipped with 512K bytes of video memory, which supports standard VGA resolutions and SVGA resolutions up to 800 x 600 in 256 colors and up to 1024 x 768 in 16 colors, interlaced or non-interlaced (CRT).

The controller includes a PC-compatible video BIOS stored in Flash EPROM. The Flash EPROM can easily be reprogrammed with BIOSes customized for a wide variety of flat-panel displays.

VGA/CRT INTERFACE

The VGA/CRT video signals are brought out to J9, a 10-pin dual-row ribbon cable connector. Most PC-compatible multi-frequency monitors require a DE15 connector. Pinouts for J9 and a DE15 connector are shown in Table 16.

J20	Signal	DE15 Pin
1	Red	1
3	Green	2
5	Blue	3
7	Horizontal Sync	13
9	Vertical Sync	14
2, 4, 6, 8, 10	Ground	5, 6, 7, 8, 10
	No Connection	4, 9, 11, 12, 15

Table 16. CRT Connector, J20

FLAT-PANEL INTERFACE

Signals for a wide range of flat-panel displays, both color and gray scale, appear on connectors J1 and J5. These connectors are designed to interface to a “daughter card,” which in turn interfaces to a particular panel or family of panels. A daughter card provides for any additional circuitry that may be needed, such as contrast control logic, backlight power connections, Vee power supply converters, power sequencing and management circuits, and for the panel’s specialized ribbon-cable connectors.

Table 17 and Table 18 list the signals on J1 and J5 respectively. A full set of flat-panel signals are provided. Note that current flat panels do not share a standardized connector pin configuration. Even the names of panel control signals vary from manufacturer to manufacturer. Review the manufacturer’s documentation to ascertain what signals are required to drive the flat panel you choose.

Pin	Signal Name	Description	Pin	Signal Name	Description
1	P4	Data 4	2	P5	Data 5
3	Gnd	Ground	4	P6	Data 6
5	P7	Data 7	6	Gnd	Ground
7	P8	Data 8	8	P9	Data 9
9	Gnd	Ground	10	P10	Data 10
11	P11	Data 11	12	Gnd	Ground
13	P12	Data 12	14	P13	Data 13
15	Gnd	Ground	16	P14	Data 14
17	P15	Data 15	18	Gnd	Ground
19	P16	Data 16	20	P17	Data 17
21	Gnd	Ground	22	P18	Data 18
23	P19	Data 19	24	Gnd	Ground
25	P20	Data 20	26	P21	Data 21
27	Gnd	Ground	28	P22	Data 22
29	P23	Data 23	30	Gnd	Ground

Table 17. Flat-Panel Interface Connector, J1

Pin	Signal Name	Description	Pin	Signal Name	Description
1	+12 V	+12 V Power	2	+12 V	+12 V Power
3	DA CS	Serial EEPROM Chip Select 1*	4	ENABKL	Enable backlight power
5	ENAVEE	Enable Vee. Power sequencing control	6	+5 V	+5 V Power
7	FLM	First Line Marker. Flat panel equivalent of VSYNC	8	ENAVDD	Enable Vdd. Power sequencing control
9	LP	Latch Pulse. Flat panel equivalent of HSYNC.	10	+5 V	+5 V Power
11	M	Sometimes called AC Drive, BLANK, or Display Enable (DE).	12	Gnd	Ground
13	SHFCLK	Shift Clock. Pixel clock for flat panel data	14	Gnd	Ground
15	P0	Data 0	16	P1	Data 1
17	Gnd	Ground	18	P2	Data 2
19	P3	Data 3	20	Gnd	Ground
21	EE DO	Serial EEPROM Data Out*	22	EE DI	Serial EEPROM Data In*
23	EE SK	Serial EEPROM Clock*	24	EE CS	Serial EEPROM Chip Select 2*

Table 18. Flat-Panel Interface Connector, J5

* These signals are used to read and write EEPROMs on some flat-panel daughter cards.

FLAT-PANEL DISPLAY VOLTAGE

Current flat panels use either +5 volts or 3.3 volts. The flat-panel daughter card has an on-board voltage regulator to provide 3.3 volt control signals to a flat panel. Use jumper JP9 on the 104Card/EV to select between +5V and +3.3V signals. Install a jumper on JP9-1/2 to select +3.3 Volts or JP9-2/3 to select +5 Volts.

POWER SEQUENCING

Some LCD flat-panel displays require power sequencing to prevent damage. For example, some panels can be damaged if the Vee bias supply is applied to the panel without first powering the control and data lines. The flat-panel video controller provides control signals for sequencing the power in the proper order to protect the panel from these effects. (The video BIOS controls the sequence and timing of these signals.) The 104Card/EV supports automatic sequencing of Vdd (+5V), Vee (bias voltages typically in the range of -30V<Vee<+30V), and +12V (for an external backlight power inverter). Use the ENAVDD and ENAVEE signals to switch the Vdd and Vee voltages respectively. Use ENABKL to control power to a backlight.

Ethernet Controller

This section describes how to configure and connect the Ethernet LAN interface.

The setup utility for the Ethernet controller is RSET8019.EXE.

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector.

In addition, software configuration of the Ethernet interface requires that you install compatible networking software:

- Install the proper driver for the network operating system you will be running.
- Use the network operating system (NOS) client install procedure provided by your NOS software vendor and follow their instructions. The Ethernet controller on the 104Card/EV is NE2000-compliant.

CONNECTING TO THE ETHERNET CABLE

The Ethernet interface supports 10BaseT (twisted pair). The interface connector is described in this section.

TWISTED PAIR INTERFACE

The twisted pair interface (10BaseT) appears on connector J17. J17 is a 5 pin single row connector with 2mm spacing. The following table lists the signals and pin numbers of J17 and the corresponding pin numbers on a RJ45 connector:

J17 Pin	Function	RJ45 Pin
1	+ Transmit Data	1
2	- Transmit Data	2
3	+ Receive Data	3
4	N/C	
5	- Receive Data	6

Table 19. Ethernet Connector, J17

CompactFlash Removable Solid-State Disk

A connector is provided for a CompactFlash (CF) card. Connected to the IDE bus, the CF cards can provide from 2M to 60M bytes or more of removable solid-state disk storage.

If you use the CF drive, it takes the place of an IDE hard disk drive in your system. Use Setup to configure your system for the IDE drives you use. Details about how to use Setup are provided in the *OEMmodule Data Book*.

The CF drive can be either an IDE master or slave. To boot from the CF drive, it must be formatted as a bootable drive and configured as master. To allow the system to boot from an IDE disk drive, the CF drive must be configured as slave. Install a jumper on JP2-1/2 to select the CF drive as master or JP2-2/3 to select the CF drive as slave.

Watchdog Timer

A watchdog timer is a circuit designed to either reset, cause an interrupt, or initiate some other recovery action if your program or hardware does not indicate that it is running properly. It usually is implemented for processes or activities that have some time predictability, such as the length of time it takes to perform a particular software function or complete the movement (or other change) of some physical system. For more information on the watchdog time, see the OEMmodule 486 databook.

A typical application, for example, would initialize the watchdog timer when certain software functions start and end, or when a limit switch or optical interrupter connected to one of the digital I/O pins changes state. If the software crashes or gets stuck in a loop, or if the mechanical switch is not closed, the watchdog timer times out, causing a system reset.

The 104Card/EV has a built-in circuit that can generate a timeout after 1.6 seconds unless reset by its input signal, WDI. WDI is an internally-generated logic signal controlled by a BIOS call. As long as the timer is reset every 1.6 seconds or less, its output signal, WDO remains in its inactive state. Should the timer time out, the WDO signal goes high, triggering a reset.

PC/104 Expansion Bus Interface

Table 20 through Table 23 document the PC/104 expansion bus provided on the 104Card/EV. It also includes the pin designations for the standard ISA expansion bus interface signals for reference to standard PC bus expansion cards.

PC/104 P1A	ISA	Signal Name	Function	In/out
A1	A1	IOCHCK-	Bus NMI input	In
A2	A2	SD7	System Data bit 7	I/O
A3	A3	SD6	System Data bit 6	I/O
A4	A4	SD5	System Data bit 5	I/O
A5	A5	SD4	System Data bit 4	I/O
A6	A6	SD3	System Data bit 3	I/O
A7	A7	SD2	System Data bit 2	I/O
A8	A8	SD1	System Data bit 1	I/O
A9	A9	SD0	System Data bit 0	I/O
A10	A10	IOCHRDY	Processor Ready Ctrl	In
A11	A11	AEN	Address Enable	I/O
A12	A12	SA19	Address bit 19	I/O
A13	A13	SA18	Address bit 18	I/O
A14	A14	SA17	Address bit 17	I/O
A15	A15	SA16	Address bit 16	I/O
A16	A16	SA15	Address bit 15	I/O
A17	A17	SA14	Address bit 14	I/O
A18	A18	SA13	Address bit 13	I/O
A19	A19	SA12	Address bit 12	I/O
A20	A20	SA11	Address bit 11	I/O
A21	A21	SA10	Address bit 10	I/O
A22	A22	SA9	Address bit 9	I/O
A23	A23	SA8	Address bit 8	I/O
A24	A24	SA7	Address bit 7	I/O
A25	A25	SA6	Address bit 6	I/O
A26	A26	SA5	Address bit 5	I/O
A27	A27	SA4	Address bit 4	I/O
A28	A28	SA3	Address bit 3	I/O
A29	A29	SA2	Address bit 2	I/O
A30	A30	SA1	Address bit 1	I/O
A31	A31	SA0	Address bit 0	I/O
A32		GND	Ground	N/A

Table 20. PC/104 Expansion Bus Connector, A1 – A32

PC/104 P1B	ISA	Signal Name	Function	In/out
B1	B1	GND	Ground	N/A
B2	B2	RESETDRV	System reset signal	Out
B3	B3	+5V	+5 volt power	N/A
B4	B4	IRQ9	Interrupt request 9	In
B5	B5	-5V		N/A
B6	B6	DRQ2	DMA request 2	In
B7	B7	-12V		N/A
B8	B8	0WS- (1)	Zero wait state	In
B9	B9	+12V		N/A
B10	B10			
B11	B11	SMEMW-	Mem Write (lower 1MB)	I/O
B12	B12	SMEMR-	Mem Read (lower 1MB)	I/O
B13	B13	IOW-	I/O Write	I/O
B14	B14	IOR-	I/O Read	I/O
B15	B15	DACK3- (1)	DMA Acknowledge 3	Out
B16	B16	DRQ3 (1)	DMA Request 3	In
B17	B17	DACK1-	DMA Acknowledge 1	Out
B18	B18	DRQ1	DMA Request 1	In
B19	B19	REFRESH- (1)	Memory Refresh	I/O
B20	B20	SYSCLK	System clock (8 MHz)	Out
B21	B21	IRQ7	Interrupt Request 7	In
B22	B22	IRQ6	Interrupt Request 6	In
B23	B23	IRQ5	Interrupt Request 5	In
B24	B24	IRQ4	Interrupt Request 4	In
B25	B25	IRQ3	Interrupt Request 3	In
B26	B26	DACK2-	DMA Acknowledge 2	Out
B27	B27	TC	DMA Terminal Count	Out
B28	B28	BALE	Address latch enable	Out
B29	B29	+5V	+5 volt power	N/A
B30	B30	OSC	14.318 MHz clock	Out
B31	B31	GND	Ground	N/A
B32		GND	Ground	N/A

(1) These signals are not supported.

Table 21. PC/104 Expansion Bus Connector, B1 – B32

PC/104 P2C	ISA	Signal name	Function	In/out
C0		GND	Ground	N/A
C1	C1	SBHE-	Bus High Enable	I/O
C2	C2	LA23	Address bit 23	I/O
C3	C3	LA22	Address bit 22	I/O
C4	C4	LA21	Address bit 21	I/O
C5	C5	LA20	Address bit 20	I/O
C6	C6	LA19	Address bit 19	I/O
C7	C7	LA18	Address bit 18	I/O
C8	C8	LA17	Address bit 17	I/O
C9	C9	MEMR-	Memory Read	I/O
C10	C10	MEMW-	Memory Write	I/O
C11	C11	SD8	System Data bit 8	I/O
C12	C12	SD9	System Data bit 9	I/O
C13	C13	SD10	System Data bit 10	I/O
C14	C14	SD11	System Data bit 11	I/O
C15	C15	SD12	System Data bit 12	I/O
C16	C16	SD13	System Data bit 13	I/O
C17	C17	SD14	System Data bit 14	I/O
C18	C18	SD15	System Data bit 15	I/O
C19		GND	Ground	N/A

Table 22. PC/104 Expansion Bus Connector, C0 – C19

PC/104 P2D	ISA	Signal Name	Function	In/out
D0		GND	Ground	N/A
D1	D1	MEMCS16-	16-bit memory access	In
D2	D2	IOCS16-	16-bit I/O access	In
D3	D3	IRQ10 (1)	Interrupt Request 10	In
D4	D4	IRQ11 (1)	Interrupt Request 11	In
D5	D5	IRQ12 (1)	Interrupt Request 12	In
D6	D6	IRQ15 (1)	Interrupt Request 15	In
D7	D7	IRQ14	Interrupt Request 14	In
D8	D8	DACK0- (1)	DMA Acknowledge 0	Out
D9	D9	DRQ0 (1)	DMA Request 0	In
D10	D10	DACK5- (1)	DMA Acknowledge 5	Out
D11	D11	DRQ5 (1)	DMA Request 5	In
D12	D12	DACK6- (1)	DMA Acknowledge 6	Out
D13	D13	DRQ6 (1)	DMA Request 6	In
D14	D14	DACK7- (1)	DMA Acknowledge 7	Out
D15	D15	DRQ7 (1)	DMA Request 7	In
D16	D16	+5V	+5 volt power	N/A
D17	D17	MASTER- (1)	Bus master assert	In
D18	D18	GND	Ground	N/A
D19		GND	Ground	N/A

(1) These signals are not supported.

Table 23. PC/104 Expansion Bus Connector, D0 – D19

BIOS Setup

The 104Card/EV system BIOS (Basic Input Output System) supports a standard Setup function to configure system parameters (as well as advanced methods specifically designed for embedded systems — refer to the OEMmodule Data Book for details). The BIOS uses the Setup parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Setup parameters are normally stored in the CMOS configuration memory, a portion of the real-time-clock circuit. In the OEMmodule, the configuration data is also stored in an internal Flash memory device. Therefore, if there is no clock battery present in the system, or if the battery fails, configuration data is not lost when power is turned off. The BIOS automatically loads configuration values from the Flash copy of the data.

Note: If you do not use a battery in your system, leave the battery input open.

USING SETUP

To enter the Setup function, press the <Del> key during POST. <Del> can be asserted at any time prior to boot.

Note: When you change Setup parameters, the new values do not take effect until the system is rebooted.

There are three Setup screens:

- **Main Menu Screen** — Displays a top-level menu of Setup choices
- **Basic CMOS Configuration** — Displays the standard CMOS options you can set for your system.
- **Custom Configuration** — Displays the custom CMOS options you can set for your system.

For details about how to set the various parameters using Setup, refer to the OEMmodule Data Book.

Specifications

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Voltage on any pin, with respect to Ground ..... -0.3V to +6.5V

Storage Temperature (case) .....-55°C to +80°C (-67°F to +176°F)

OPERATING CONDITIONS*

Supply Voltage (V_{CC}) .....4.75V to +5.25V

Case Temperature (under bias) .....0°C to 70°C (32°F to 158°F)

* Stresses above those listed above can cause permanent damage to the board. These values are stress ratings only and do not imply that the device should be operated at these extremes. Exposure beyond the "Operating Conditions" may affect device reliability. Note that some power supplies exhibit voltage spikes when AC power is switched on or off or when voltage transients appear on the AC power line. If this possibility exists it is suggested that you use a clamp circuit on the DC supply.

Literature References

The following references are for information about the PC architecture, the 386SX microprocessor, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson

Internet: mindshar@interserv.com

CompuServe: 72507,1054

Published by Addison Wesley, Inc.

http://www.mindshare.com

AT Bus Design

Edward Solari

Anabooks

12145 Alta Carmel Ct., Suite 250

San Diego, CA 92128

ISBN 0-929392-08-6

http://www.anabooks.com/

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.

445 Hoes Lane

Piscataway, NJ 08854

http://www.ieee.org/

MS-DOS References

MS-DOS Functions, Ray Duncan, Microsoft Press

MS-DOS Programmer's Reference, Microsoft Press, Microsoft Corporation

Undocumented DOS, Andrew Schulmen, Addison/Wesley

Technical data on the 486SX microprocessor:

486SX Microprocessor Programmer's Reference Manual

Intel

1751 Fox Drive

Suite 29000

San Jose, CA 95131

http://www.intel.com/

Technical data on Embedded DOS 6-XL

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The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0

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MANUAL REVISIONS

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All	Revision A	3/18/99

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